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STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,147	TAGO ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Henry (patent No. 6,550,004) in view of Shiell (patent No. 6,108,775 and McFarling (patent no. 6,374,349).

In regard to claim 1,

a. Henry has disclosed an apparatus for branch prediction, comprising:

i. a history register (figures 2, and 3, element 216) which stores therein history of previous branch instructions;

ii. an index generation circuit which generates a first index from an instruction address and the history stored in said history register (figure 3, element 312);

iii. a history table (figure 3, element 302) which stores therein a portion of the instruction address as a tag and a first value indicative of a likelihood of branching in association with the first index; [column 8, lines 31-40 show that that the history table is indexed by a hash value equal to a modified portion of the address, or a tag. Lines 50-55 show that the table also holds an Agree/Disagree bit. Lines 21-30 show that this bit is

used to make a branch prediction or determine the likelihood a branch is taken.]

iv. a buffer indicated by the instruction address and a address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address; Figures 2 and 3 and the sections cited above show that a second dynamic branch predictor(element 204) is used to indicate and store (thus a buffer) the likelihood of a branch being taken and is indexed by a function of a portion of the instruction address.

v. and a selection unit which makes a branch prediction by selecting one of the first value and the second value (figure 2, element 206.)

b. Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of and instruction.

c. Shiell disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d. Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the

prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the design of Henry to use the branch destination buffer of Shiell as a dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

As to the limitation of a tag (claim 1) that is a portion of the instruction address McFarling taught this limitation (e.g., see col. 7, lines 41-65) [a branch history cache stores tags that comprise a portion of branch whose history is stored in the history entry.] (in system that predicts branches (e.g., see col. 7, lines 1-65).

As to the counter limitation of claim 1, McFarling taught a count value indicative of a likelihood of branching in association with a first index (e.g., see fig. 12,14 and col. 3, lines 1-58)[when the count is in the upper range (10 or 11) it predicts that a branch will be taken; a count in the lower half (00 or 01) predicts that it will not be taken].

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Henry and McFarling. McFarling taught a system provided a system for accurately predicting the outcome of conditional branches. One of ordinary skill would have been motivated to incorporate the McFarling teachings of counters for increasing the accuracy of dynamic predictions into the Henry system at least to increase the

accuracy of branch prediction (e.g., see fig. 20 and col. 1, line 60-col. 6, line 14 of McFarling).

3. In regard to claim 2, Henry in view of Shiell discloses the apparatus as claimed in claim 1, wherein a) said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has an entry therein corresponding to the current instruction address and current history;[Figure 5, case 1 shows that the X predictor (history table) is selected (selector agrees (A) with the static prediction X) when both X and Y (BTB) are correct and thus they both must have a corresponding value.] b) and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history. [Figure 5, case 11 shows that the X (table) predictor was wrong and the Y (BTB) predictor was correct. Thus the Y predictor had a corresponding entry and the X predictor either had a wrong value or did not have an entry of which give a wrong predictor. In this case the BTB was selected.]

4. In regard to claim 3, Henry in view of Sheill discloses the apparatus as claimed in claim 2, wherein said selection unit predicts no branching if said branch destination buffer does not have and entry therein corresponding to the current instruction address. [Figure 5, cases 13-16 of Henry illustrates when both predictors are wrong, which includes the case where neither have a corresponding entry. Here the static prediction is either agreed or disagreed with and as shown throughout the disclosure the

prediction is either "taken" or "not taken" and thus there are instances where the prediction is not taken.

5. In regard to claim 4, Henry in view of Shiell discloses the apparatus claimed in claim 1, wherein said index generation circuit generates the first index that is an Exclusive-OR between the history stored in said history register and the current instruction address (figure 3).

6. In regard to claim 5,

a) Henry in view of Shiell discloses the apparatus as claimed in claim 1;

b) Henry in view of Shiell does not disclose wherein more than one said history table is provided so as to allow a plurality of entries to be registered with respect to said first index;

c) While a plurality of history tables is not explicitly taught, a single history table is taught as shown above, The inclusion of a plurality of history tables to perform the same claimed function as a single history table provides no new of unexpected result over the prior art. Therefore one of ordinary skill in the art would have found it obvious t duplicate the fetch module, creating a fetch module for each pipeline. With multiple duplicate history tables in place, multiple entries in the multiple tables would inherently be allowed to be registered with the same index since each is a duplicate (see MPEP 2144.04 (VI): In re Harza, 274 F.2d. 669,671, 124 USPQ 378,380,(CCPA) 1960)).

7. In regard to claim 6,

a. Henry in view of Shiell discloses a processor (figure 1), comprising:

I) a history register (figures 2 and 3, element 216) which stores therein history of previous branch instructions ;

II) and index generation circuit (figure 3, element 312) which generates a first index from an instruction address and the history stored in said history register;

III) a history table (figure 3, element 302) which stores therein a portion of the instruction address as a tag and a first value indicative of likelihood of branching in association with the first index; [Column 8, lines 31-40 show that the history table is indexed by a hash value equal to a modified portion of the address, or a tag. Lines 50-55 show that this bit is used to make a branch prediction or determine the likelihood a branch is taken.]

IV) a buffer inidicated by the instruction address and a second value indicative of likelihood of branching in association with a second index that is at least a portion of the instruction address; Figures 2 and 3 and the sections cited above show that a second dynamic branch predictor (element 204) is used to indicate and store (thus a buffer) the likelihood of a branch being taken and is indexed by a function of a portion of the instruction address.

V) a selection unit which makes a branch prediction by selecting one of the first value and the second value (figure 2 , element 206);

VI) an execution control unit which controls execution of instructions and a execution operation unit (figure 1, element 109) which executes the instructions. [The execution unit inherently has control logic to control it.]

b. Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction;

c. Shiell disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination of target address of an instruction and is indexed by tags (portion of the instruction address) as disclosed in column 2, lines 12-34).

d. Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated on of ordinary skill in the art to modify the design of Henry to use the branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the design of Henry to use branch destination buffer of Shiell as the dynamic

branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

As to the limitation of a tag (claim 6) that is a portion of the instruction address McFarling taught this limitation (e.g., see col. 7, lines 41-65) [a branch history cache stores tags that comprise a portion of branch whose history is stored in the history entry.] (in system that predicts branches (e.g,. see col. 7, lines 1-65).

As to the counter limitation of claim 6, McFarling taught a count value indicative of a likelihood of branching in association with a first index (e.g., see fig. 12,14 and col. 3, lines 1-58)[when the count is in the upper range (10 or 11) it predicts that a branch will be taken; a count in the lower half (00 or 01) predicts that it will not be taken].

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Henry and McFarling. McFarling taught a system provided a system for accurately predicting the outcome of conditional branches. One of ordinary skill would have been motivated to incorporate the McFarling teachings of counters for increasing the accuracy of dynamic predictions into the Henry system at least to increase the accuracy of branch prediction (e.g., see fig. 20 and col. 1, line 60-col. 6, line 14 of McFarling).

8. In regard to claim 7,

a. Henry in view of Shiell discloses a method of branch prediction comprising the steps of:

i. providing a history table (figure 3, element 302) which stores therein a portion of the instruction address as a tag and a first value indicative of a likelihood of branching in association with the first index that is generated from the instruction address and history of previous branch instructions; [column 8, lines 31-40 show that that the history table is indexed by a hash value equal to a modified portion of the address, or a tag.
Lines 50-55 show that the table also holds an Agree/Disagree bit. Lines 21-30 show that this bit is used to make a branch prediction or determine the likelihood a branch is taken.]

ii. providing a buffer (interpreted as hardware as indicated in the specification in order to avoid 35 USC 101 problems) indicated by the instruction address and a address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address; Figures 2 and 3 and the sections cited above show that a second dynamic branch predictor(element 204) is used to indicate and store (thus a buffer) the likelihood of a branch being taken and is indexed by a function of a portion of the instruction address.

iii. an predicting branching in response to the selected one of the first value and the second value (figure 2, element 189 gives T for taken or NT for not taken).

b. Henry has not disclosed the buffer being a branch destination buffer which stores a branch destination address or predicted branch destination address of an instruction;

c. Shiell disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d. Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the design of Henry to use the branch destination buffer of Shiell as a dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

9. As to the limitation of a tag (claim 7) that is a portion of the instruction address McFarling taught this limitation (e.g., see col. 7, lines 41-65) [a branch history cache

stores tags that comprise a portion of branch whose history is stored in the history entry..] (in system that predicts branches (e.g., see col. 7, lines 1-65).

As to the counter limitation of claim 7, McFarling taught a count value indicative of a likelihood of branching in association with a first index (e.g., see fig. 12,14 and col. 3, lines 1-58)[when the count is in the upper range (10 or 11) it predicts that a branch will be taken; a count in the lower half (00 or 01) predicts that it will not be taken].

It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Henry and McFarling. McFarling taught a system provided a system for accurately predicting the outcome of conditional branches. One of ordinary skill would have been motivated to incorporate the McFarling teachings of counters for increasing the accuracy of dynamic predictions into the Henry system at least to increase the accuracy of branch prediction (e.g., see fig. 20 and col. 1, line 60-col. 6, line 14 of McFarling).

10. In regard to claim 8, Henry in view of Shiell discloses the method as claimed in claim 7, wherein,

a. said step of selecting one of the first value and the second value selects the first value if said branch destination buffer has an entry therein corresponding to the current instruction address and said current history table has an entry therin corresponding to the current instruction address and current history ;[Figure 5, case 1 shows that the X predictor (history table) is selected (selector agrees (A)

with the static prediction X) when both X and Y (BTB) are correct and thus they both must have a corresponding value.]

b. and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history. [Figure 5, case 11 shows that the X (table) predictor was wrong and the Y (BTB) predictor was correct. Thus the Y predictor had a corresponding entry and the X predictor either had a wrong value or did not have an entry of which give a wrong predicton. In this case the BTB was selected.]

11. In regard to claim 9, Henry in view of Shiell discloses the method as claimed in claim 8, further comprising the steps of:

a. registering the current instruction address in said branch destination buffer if said branch destination buffer does not have an entry therein corresponding to the current instruction address ((Shiell , column 2, lines 28-34);

b. and registering information about the current instruction address in the history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have and entry therein corresponding to the current instruction address and the current history and if a prediction made based on the second value turns out to be erroneous. [This above cited section also shows that current entries are modified based on the branch outcome, including times when there was an erroneous prediction. This happens regardless of the other table, so the update occurs at time when there is no entry in the history table.]

12. In regard of claim 10, Henry in view of Shiell discloses the method as claimed in claim 9 wherein the information about the current instruction address is not registered in said history table if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history and if the prediction made based on the second value turns out to be correct. [Figure 5 of Shiell shows cases (10 and 11 for example) where the BTB (Y) prediction was correct and the history table (X) was incorrect (which includes if it does not have an entry since it thus cannot be correct) and where the history table (X) was not updated.]

13. In regard to claim 11,

a. Henry in view of Shiell discloses an apparatus for branch prediction comprising:

i. a history register (figures 2, and 3, element 216) which stores therein history of immediately preceding branch instructions;

ii. an index generation circuit which generates a first index that is an Exclusive-OR between an instruction address and the history stored in said history register (figure 3, element 312);

iii. a history table (figure 3, element 302) which stores therein a portion of the instruction address as a tag and a first value indicative of a likelihood of branching in association with each said first index; [column 8, lines 31-40 show that that the history table is indexed by a hash value equal to a modified portion of the address, or a tag. Lines 50-55 show that

the table also holds an Agree/Disagree bit. Lines 21-30 show that this bit is used to make a branch prediction or determine the likelihood a branch is taken.]

iv. a buffer indicated by the instruction address and a second value indicative of a likelihood of branching in association with a second index that is at least a portion of the instruction address; Figures 2 and 3 and the sections cited above show that a second dynamic branch predictor(element 204) is used to indicate and store (thus a buffer) the likelihood of a branch being taken and is indexed by a function of a portion of the instruction address.

v. and a selection unit (figure 2, element 206.) which makes a branch prediction by selecting one of the first value and the second value, wherein said selection unit selects the first value if said branch destination buffer has an entry therein corresponding to a current instruction address and said history table has and entry therein corresponding to the current instruction and said instruction address and current history, and selects the second value if said branch destination buffer has an entry therein corresponding to the current instruction address and said history table does not have an entry therein corresponding to the current instruction address and the current history. [Figure 5, case 1 shows that the X predictor (history table) is selected (selector agrees (A) with the static predictor (history table) is selected (selector agrees (A) with the static

prediction X) when both X and Y (BTB) are correct and thus they both must have a corresponding value. Figure 5, case 11 shows that the X(table) predictor was wrong and the Y (BTB) predictor was correct. Thus the Y predictor had a corresponding entry and the X predictor either had a wrong value or did not have an entry both of which give a wrong prediction. In this case the BTB was selected.]

b. Henry has not disclosed the buffer being a branch destination buffer which stores therein a branch destination address or predicted branch destination address of an instruction;

c. Shiell disclosed the use of a dynamic branch predictor that is a branch destination buffer or branch target buffer that stores a branch destination or target address of an instruction and is indexed by tags (portion of the instruction address) as discussed in column 2, lines 12-34.

d. Shiell has also shown in this section that this branch target buffer is more accurate than a predictor that keeps track of other branches (such as a plain history table) by keeping track of each branch's history. In addition, by storing the target address, the destination may be fetched immediately based on the prediction without calculating the instruction address and thus instruction fetching is quicker. The ability to have more accurate branch prediction and speed up instruction fetching would have motivated one of ordinary skill in the art to modify the design of Henry to use branch destination buffer taught by Shiell as the dynamic branch predictor (element 204) of Henry.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the design of Henry to use the branch destination buffer of Shiell as a dynamic branch predictor 204 of Henry so that more accurate prediction is used and instruction fetching is sped up.

14. As to the limitation of a tag (claim 10) that is a portion of the instruction address McFarling taught this limitation (e.g., see col. 7, lines 41-65) [a branch history cache stores tags that comprise a portion of branch whose history is stored in the history entry.] (in system that predicts branches (e.g., see col. 7, lines 1-65).

15. As to the counter limitation of claim 10, McFarling taught a count value indicative of a likelihood of branching in association with a first index (e.g., see fig. 12,14 and col. 3, lines 1-58)[when the count is in the upper range (10 or 11) it predicts that a branch will be taken; a count in the lower half (00 or 01) predicts that it will not be taken].

16. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Henry and McFarling. McFarling taught a system provided a system for accurately predicting the outcome of conditional branches. One of ordinary skill would have been motivated to incorporate the McFarling teachings of counters for increasing the accuracy of dynamic predictions into the Henry system at least to increase the accuracy of branch prediction (e.g., see fig. 20 and col. 1, line 60-col. 6, line 14 of McFarling).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 12, 13 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by McFarling (patent No. 5,374,349).

17. As per claim 12, McFarling taught correlating a tag representing a part of a branch instruction address for the instruction with a count value indicative of a likelihood of branching occurring; and comparing said tag with an index to assist in determining whether branching should occur on said count value (e.g., see fig. 5,12,14,20 and col. 10, lines 14-col. 11, line 15) and col. 11, line 16-col. 12, line 5) [a prediction is made using a branch address and count value and doing the same procedure for several stages and comparing the prediction to determine if predictions agree for determining if branching should occur] .

18. As per claim 13, McFarling taught an XOR circuit adapted to perform and XOR operation on a portion of a branch instruction address and contents of a history register to generate an index; a comparison unit adapted to compare said index with a tag representing a portion of an instruction address; and a selection unit adapted to perform a count value selection based on said comparison to determine branching of said instruction (e.g., see fig. 5,12,14, and col. 10, lines 14-65, and col. 11, line 16-col. 12, line 5).

19. As per claim 14, McFarling taught providing a correlation in which a tag representing a part of a branch instruction address is correlated with a first count value; providing a correlation in which a tag is correlated with a second value. Selecting one of said first count value and said second value to predict branching of said instruction depending upon whether an index is matched to said tag in said first correlation or said tag in said second correlation (e.g., see fig. 5,12,14,20 and col. 10, lines 14-col. 11, line 15) and col. 11, line 16-col. 12, line 5) [a prediction is made using a branch address and count value and doing the same procedure for several stages and comparing the prediction to determine if predictions agree] .

Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tran (patent No. 5,995,749) disclosed a branch prediction mechanism employing branch selectors to select a branch prediction (e.g., see abstract).

Black (patent No. 5,761,723) disclosed a data processor with branch prediction (e.g., see abstract).

Pickett (patent No. 6,101,595) disclosed a system fetching instructions fro an instruction cache using sequential way prediction (e.g., see abstract).

Col (patent No. 6,526,502) disclosed a system for speculatively updating global branch history with branch prediction prior to resolution of branch outcome (e.g., see abstract).

Keller (patent No. 6,687,789) disclosed a cache which provides partial tags from a non-predicted ways to direct search if way prediction misses (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

Eric Coleman

ERIC COLEMAN
PRIMARY EXAMINER